

Assembly Guideline for ZVS Buck and Buck-Boost 10 x 10mm and 10 x 14mm LGA/BGA Packages



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Description

This application note provides information and recommendations relevant to handling procedures and assembly with the 10 x 10 and 10 x 14 Land Grid Array (LGA) and Ball Grid Array (BGA) packages.

SiP Details

- Refer to 10 x 10 and 10x14mm Package Drawings respectively.
- All pads are SMD (solder mask defined).
- All pads are Ni/Au finish.

LGA

- All pads are 0.55 x 0.55mm (exposed copper area).
- MSL rating - MSL3 @ 245°C.

BGA

- All solder bumps are .64mm diameter.
- MSL rating - MSL3 @ 245°C.

Receiving PCB Pad

- OSP, ENIG, ENEPIG, or Ni/Au finish recommended.
- Pads within planes/polygons are SMD only, with 0.55 x 0.55mm final size solder mask openings.
- Signal pads can be either SMD or NSMD (non-solder mask defined).
- SMD signal pads should have a minimum copper pad of 0.65 x 0.65mm, with a solder mask opening of 0.55 x 0.55mm.

LGA

- All pads have exposed copper area of 0.55 x 0.55mm.
- NSMD should have a copper defined pad of 0.55 x 0.55mm, with a solder mask opening of 0.65 x 0.65mm.

BGA

- All pads have exposed copper area of 0.45mm diameter pad opening.
- NSMD should have a copper defined pad of 0.45mm diameter Cu defined/SM opening of 0.6mm.

Receiving PCB Board (LGA/BGA)

- Board should be made from FR4 – Tg 170°C or higher rated material.
- Board should have a minimum of four layers of 2oz copper.
- Planes/Polygons underneath part should not have thermal reliefs around SMD pads or vias.
- Thermal vias are recommended, please refer to specific product data sheets for information.
- Silkscreen under the SiP is not recommended.

Solder-Paste Stencil

LGA

- Recommended stencil openings for pads is 0.45 x 0.45mm (80% aperture) using a 5mil or 6mil stencil thickness.
- Aperture size should not exceed 95% to ensure paste is not in the solder mask area.

BGA

- Recommended stencil openings are .40mm diameter (90% aperture) using a 4mil or 5mil stencil thickness.
- Flux can also be used using a 2mil thick stencil.

Assembly and Cleaning

- Handling and storage of SiPs per IPC 1601, JEDS625-B
- Pre-bake components based on component MSL rating prior to assembly (per IPC/JEDEC J-STD-020D.1)
- Pick and place should be from the center of the component
- Pb or Pb free (SAC305), low voiding solder paste such as AIM WS488, Kester 520A, or equivalent
- Aqueous clean using a saponifier or ultrasonic
- DI water spray for under SiP cleaning

Inspection

- X-ray inspection is recommended for solder joint inspection
- Up to 25% area voiding per pad is acceptable

Rework and Removal

- Rework maximum temperature should not exceed 245°C (from Table 3) .
- Removed SiP should not be reused.

Moisture Sensitivity Level (MSL)

- Components are baked and dry-packed before shipment.
- Components should remain in a dry vacuum bag during storage prior to assembly.
- A MSL label is attached to the outside bag.
- Within the bag is a humidity indicator card and desiccant .
- Shelf life of the components sealed in the bag is 2 years at < 40°C and < 90% room humidity (RH).
- The MSL label indicates maximum open air exposure and bake times.
- Please reference JEDEC standard J-STD-033 for additional information.

Assembly Reflow Guidelines (LGA/BGA)

Table 1
Reflow profile
recommendations
(JEDEC/IPC J-STD-020D.1)^{[a] [b] [c]}

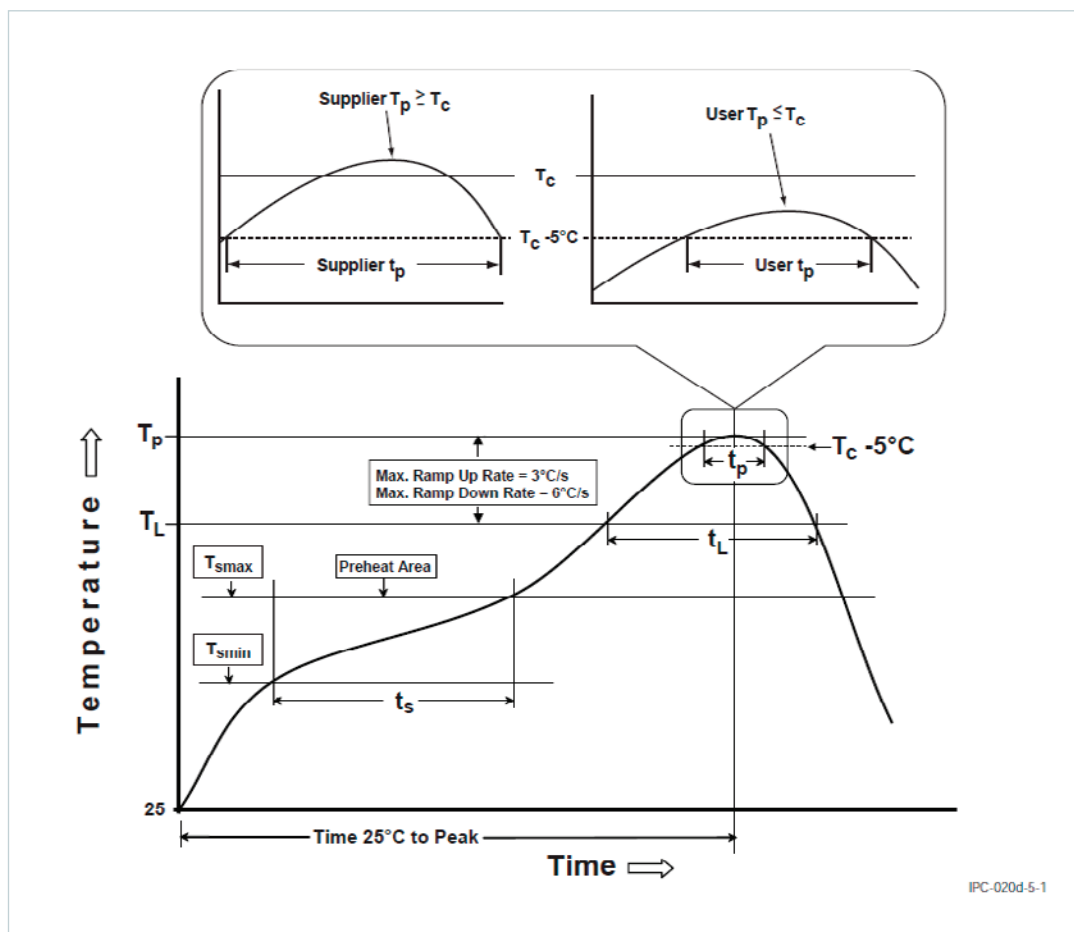
Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Pre-heat temperature Min (T_{SMIN})	100°C	150°C
Pre-heat temperature Max (T_{SMAX})	150°C	200°C
Pre-heat time (t_s) from T_{smin} to T_{sMAX}	60 – 120 seconds	60 – 120 seconds
Ramp-up Rate (T_L to T_p)	3°C/second maximum	3°C/second maximum
Liquidus temperature (T_L)	183°C	217°C
Time (t_L) maintained above T_L	60 – 150 seconds	60 – 150 seconds
Peak package body temperature (T_p)	220°C	245°C
Time (t_p) within 5°C of peak temperature (T_p)	20 seconds	20 seconds
Ramp-down Rate (T_p to T_L)	6°C/second maximum	6°C/second maximum
Time 25°C to T_p	6 minutes maximum	8 minutes maximum

^[a] All temperatures refer to the topside of the package, measured at the center of the package on the body's surface.

^[b] Tolerance for T_p is defined as a supplier's minimum and a user's maximum.

^[c] Product MSL levels are defined in the product data sheet.

Figure 1
Reflow classification profile
(JEDEC/IPC J-STD-020D.1)



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