WHITE PAPER

Control of a Discontinuous-Conduction-Mode ZVS Buck-Boost Topology for Microprocessor Core Power

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Abstract

The potential for gains in efficiency, power density and performance when using discontinuous-conduction-mode (DCM) Zero-Voltage Switching (ZVS) buck-boost topology motivates the study of its use in providing microprocessor core power. In this paper, the authors navigate the design challenges one encounters implementing such a voltage regulation scheme that are not seen in the traditional continuous-conduction-mode multiphase buck topology. The model of the plant is analyzed and a control methodology is proposed. Experimental results successfully validate the performance to the Intel VR12 specification.

Introduction

Using a buck-boost topology from a 48V input followed by a broadband fixed-ratio DC-DC converter stage used as a DC transformer is a unique approach for powering processor core voltage, for which the most common implementation uses a multiphase continuous-conduction-mode buck converter from 12V.[a] [b] [c] [d] [e] While some of these topologies have offered innovative ways to improve efficiency,[d] [e] there are cases where using a higher distribution bus voltage (i.e., ETSI 48V) will greatly reduce transmission loss and further improve system efficiency.[f] [g] [h] [i] [j] [k] The low duty cycle required would make buck conversion directly from these higher bus voltages prohibitive, so a topology that includes a transformer stage is needed. Once the transformer stage is introduced, one is no longer limited to a buck-converter stage and can explore the benefits that a buck-boost converter has to offer.

There are several challenges in controlling a DCM ZVS buck-boost-based topology with an off-the-shelf control IC beyond those one encounters with a more traditional topology. First, the modulator gain of the discontinuous-conduction-mode powertrain varies with load.[l] Secondly, a ZVS buck-boost topology, when operating near full duty cycle, typically has less "overdrive" ability to respond to set point and load transients. Still, the potential for reducing transmission losses, as well as the inherently higher efficiency from running closer to full duty cycle and using zero-voltage switching, has driven the further investigation of this interesting topology.

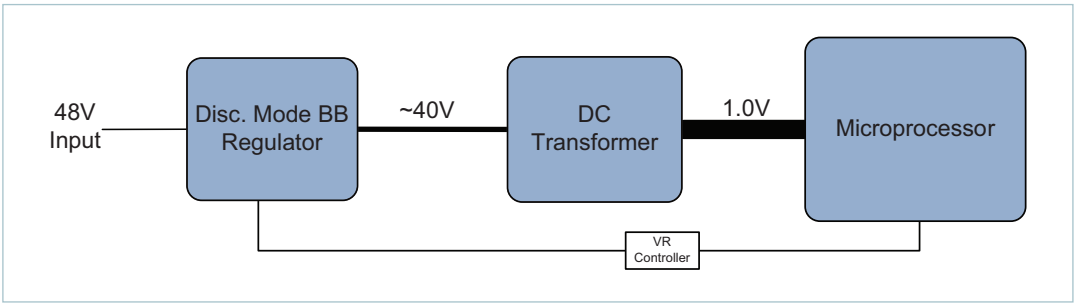
The plant

As seen in Figure 1, the plant can be analyzed in two parts:

1. The discontinuous-conduction-mode ZVS buck-boost converter
2. The DC transformer and passive filter components

The architectural concept is that the buck-boost converter acts as the dependent source while the DC transformer (though a switching component) along with the other filter components can be considered (and analyzed) as a passive filter (adding switching noise sources when necessary for analysis).

Figure 1
System block diagram



The DCM ZVS buck-boost converter

In the system depicted in Figure 1, the discontinuous-conduction-mode buck-boost converter has a load pole at:

$$f_{PL} = \frac{1}{2\pi \left(\frac{V_{OUT}}{I_{OUT}} \| \frac{r_{PT}}{N^2} \right) C_{OUT\_EQ}} \qquad (1)$$

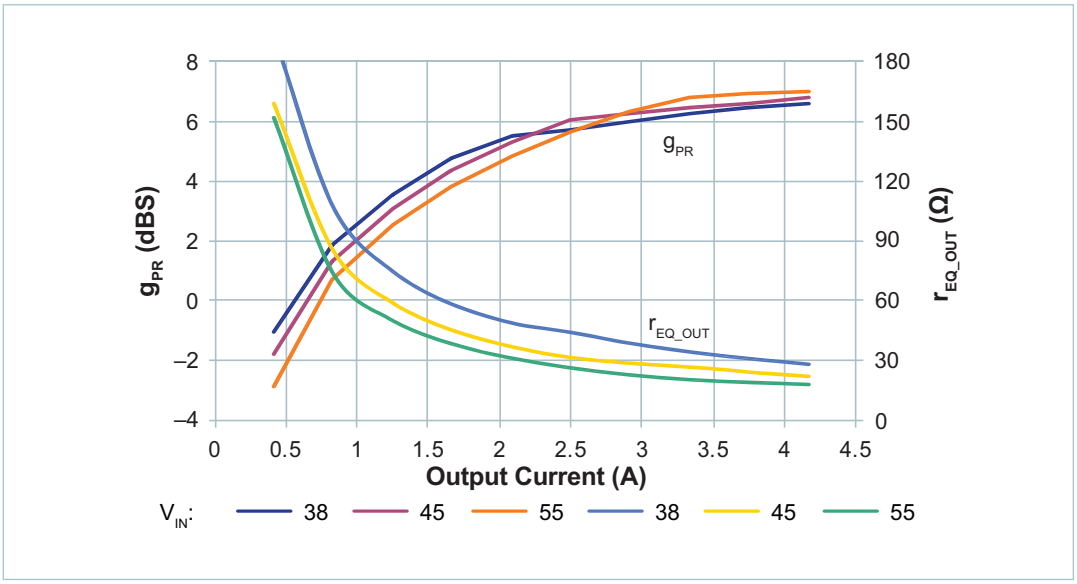
where r_{PT} is the small signal output resistance of the ZVS buck-boost, which also varies with load, V_{OUT} is the voltage at the load, I_{OUT} is the current at the load, N is the turns ratio of the DC Transformer, and C_{OUT_EQ} is the equivalent output capacitance, where the capacitance at the output of the buck boost stage (i.e., upstream of the DC transformer stage) has been multiplied by the square of the turns ratio and added to the load capacitance:

$$C_{OUT\_EQ} = C_{LOAD} + N^2 C_{OUT\_BB} \qquad (2)$$

One should note that in Equation 1, once the load current dominates, as the load increases, the frequency of the dominant pole will also increase. Because this pole is well below crossover, the main effect is to make the buck-boost act as an integrator, though one should note in systems where the modulator gain of the buck-boost is not constant, this leads to a dropoff in gain at light loads.

To optimize efficiency, the discontinuous-conduction-mode powertrain should approach critical conduction at full DC load.[m] However, this limits the ability of the powertrain to cope with set-point transients near full load. Thus an accurate analysis over different load conditions is needed. Derivation of the DC modulator gain for the discontinuous-conduction-mode buck-boost converter is described in.[l] For the purposes of this paper, we will consider the Vicor PRM48DH480T250A03 ZVS buck-boost converter.[n] The resulting modulator gain for the system is shown in Figure 2. The third section of this paper will use this modulator gain model to design the system compensation.

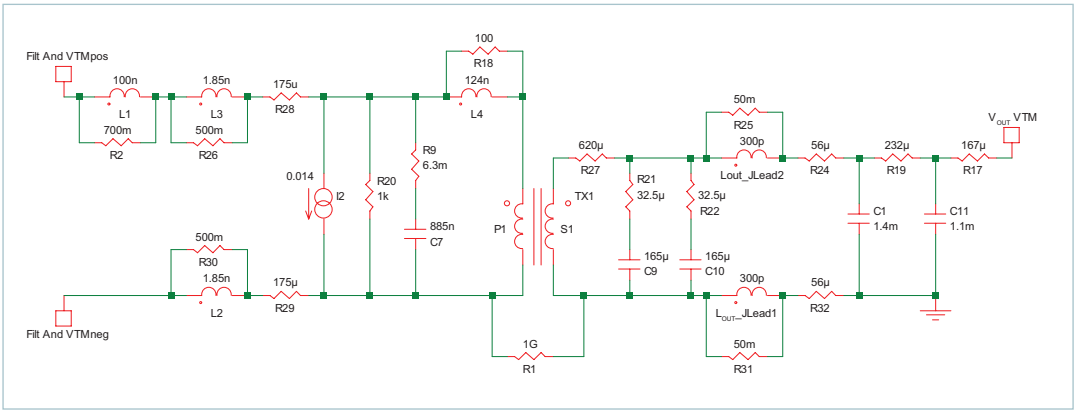
Figure 2
DC modulator gain and powertrain equivalent output resistance vs. output current, V_{OUT} = 48V



The DC transformer and passive filter

For the second "passive" portion of the plant, the following model in Figure 3 can be used. This model results in a low-pass system with multiple poles and zeros, for which a pole at 102kHz dominates. While the system can be treated as a single-pole system up to 300kHz, the system was analyzed with seven state variables, motivated by obtaining accurate gain margin estimates which occur near this frequency.

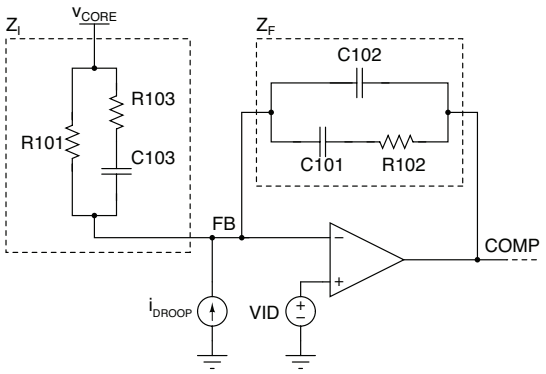
Figure 3
Model of the effectively passive portion of the plant



Compensation

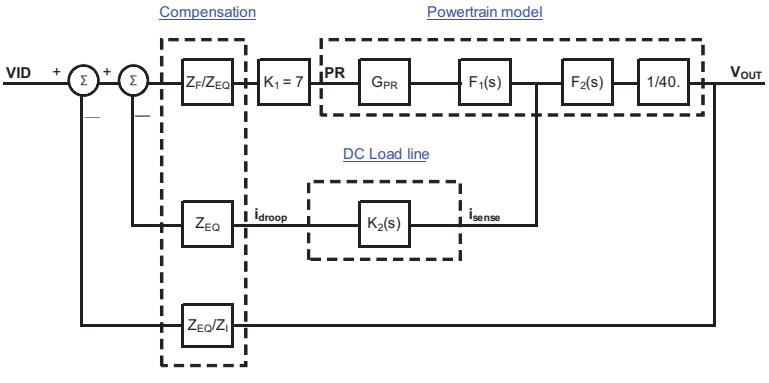
The proposed control topology is the Type III compensator (three poles, two zeros) as shown in Figure 4. Throughout the remainder of this paper, the network between the output of the compensation and the feedback node (C101, C102 and R102) will be referred to as Z_F, while the network between the system output and the feedback node (R101, R103 and C103) will be referred to as Z_I.

Figure 4
The proposed compensator



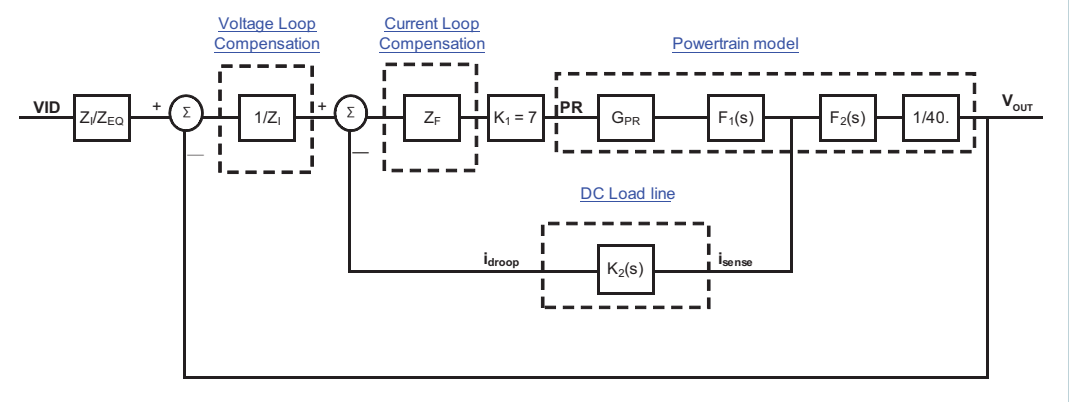
In the case of microprocessors with a load line, there are actually two interacting control loops. As shown in Figure 5, these are the current loop, which controls the output voltage droop proportional to the current, and the outer voltage loop. In the proceeding figures, Z_{EQ} refers to the parallel combination of Z_F and Z_I.

Figure 5
Model of the entire control system, showing two interacting control loops



A strategy for compensation of this plant is to first compensate the inner current loop using the first zero and the integrator (Z_F), then compensating the phase of the outer voltage loop with the remaining independent zero (Z_I) as elucidated in Figure 6. Z_I also contains R101, which sets the load line and gain of the outer loop. While the loops remain heavily coupled, the authors will show this method does allow one to find stable solutions, albeit limited in bandwidth by the current loop.

Figure 6
Control system model, rearranged to show the control strategy explicitly

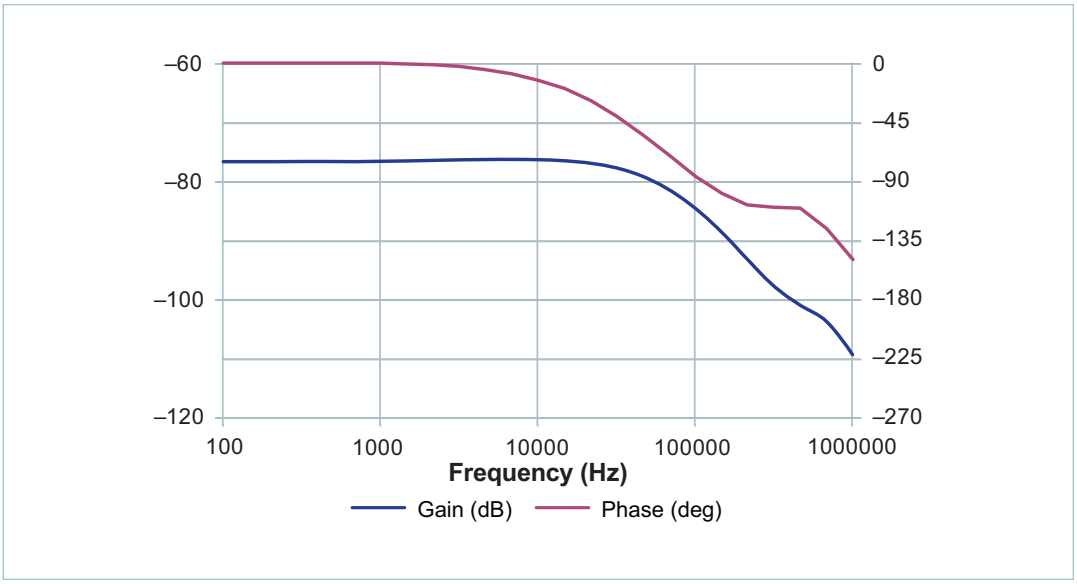


One benefit of this control method is that one can close the current loop in such a way as to compensate for the load variability of the plant response. As long as the compensated closed current loop maintains its response over the range for which the voltage loop has gain, a non-varying system response is possible, and voltage-loop compensation is simplified.

Inner-loop compensation

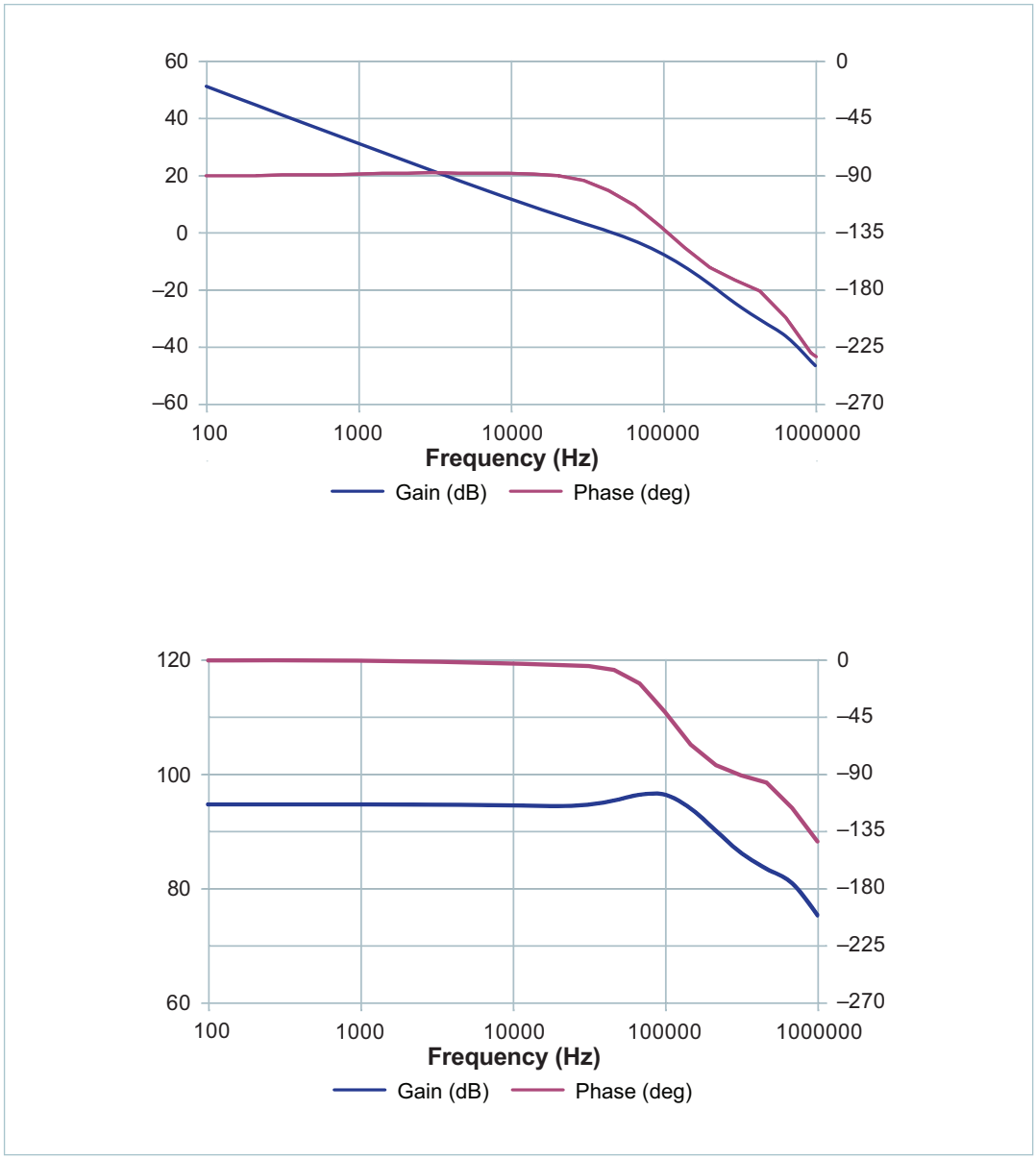
The inner loop of this system has an uncompensated loop transmission as shown in Figure 7. Because tuning the gain of the outer loop using Z_I is limited, the inner loop should be set such that it has high gain but still remains flat (i.e., the inner loop should have optimized gain margin and phase margin).

Figure 7
Uncompensated loop transmission of the inner (current) loop



A compensation is chosen with a zero at 30.2kHz, a pole at 205kHz, an integrator gainbandwidth of 14.9kHz (or, if K_1 is included as part of the compensation rather than the plant, the integrator has a gain-bandwidth of 1.04MHz). The resulting inner-loop response is shown in Figure 8.

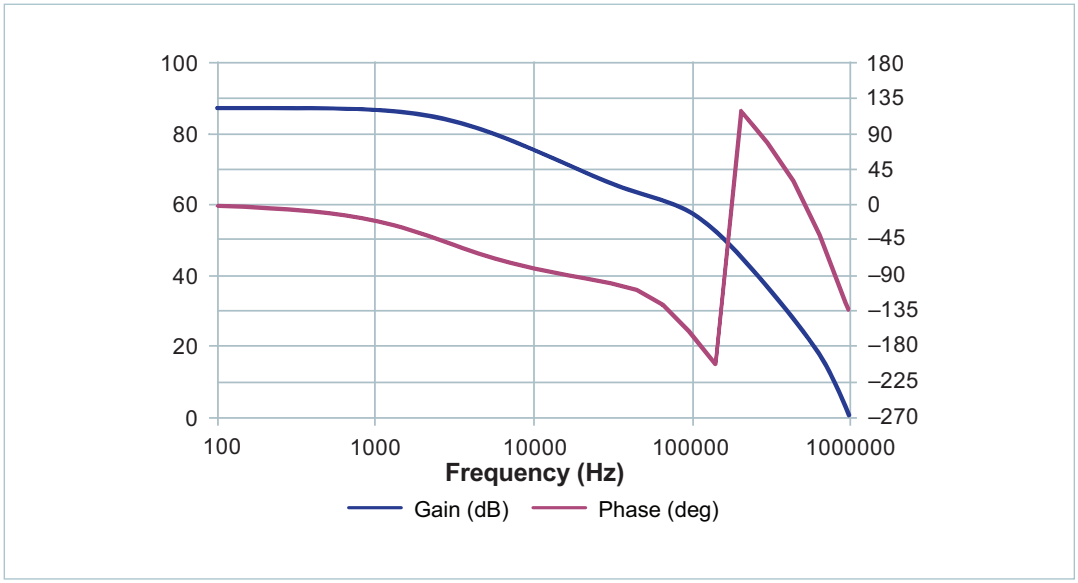
Figure 8
Compensated inner-loop transmission (top) and closed-loop response (bottom)



Outer-loop compensation

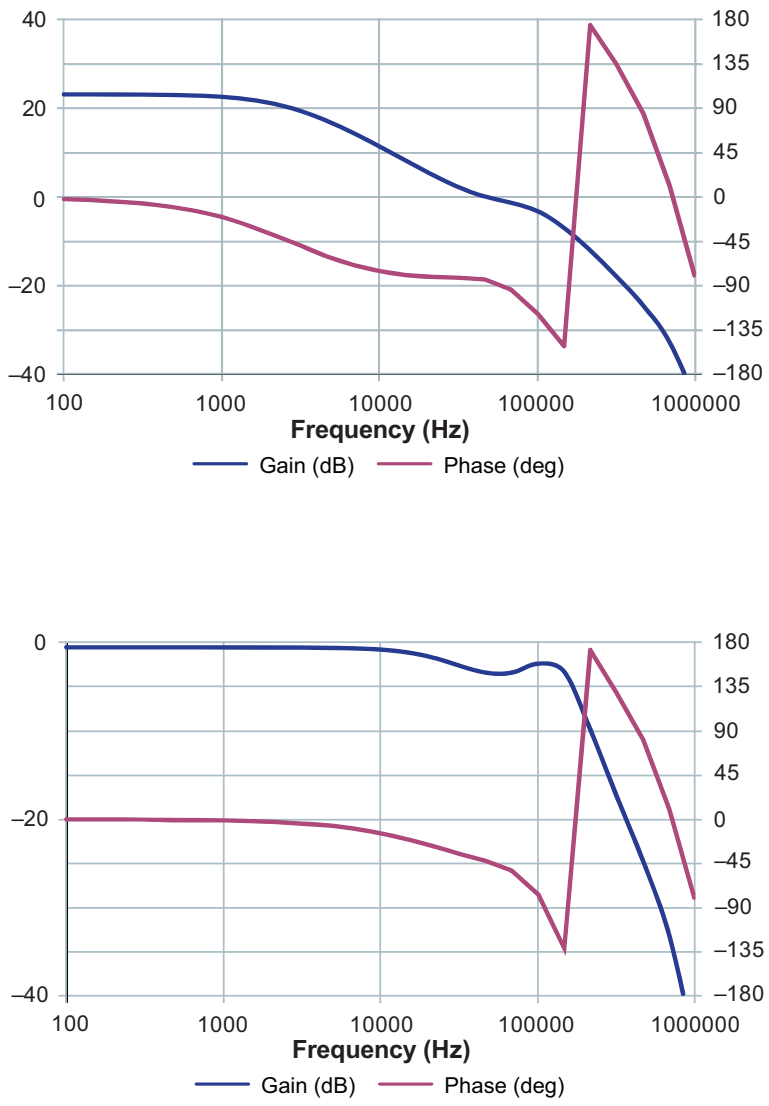
In the case of the outer voltage loop, the loop transmission to be compensated can be seen in Figure 9. Note that the gain and phase drop off rapidly at around 100kHz, therefore acheiving a loop response near 100kHz is difficult.

Figure 9
Uncompensated outer (voltage) loop transmission



In designing the compensation admittance $1/Z_l$, the resistor R101 is predetermined by the load line. It is the recommendation of the authors that one allows this resistance to determine the loop bandwidth, then uses the pole-zero pair to maximize the gain and phase margin of the system. This method was used to obtain the response in Figure 10, where the zero was placed at 90.4kHz and the pole at 1.06MHz. The model predicts that the outer loop will have a crossover bandwidth of 45kHz, a phase margin of greater than 90° and a gain margin greater than 10dB.

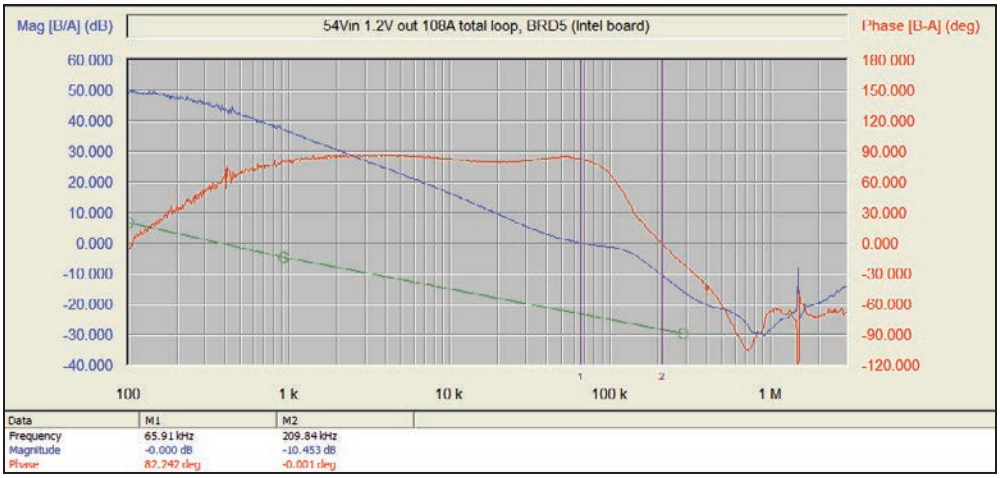
Figure 10
Compensated inner-loop transmission (top) and closed-loop response (bottom)



Results

The system described above was realized using a Vicor PRM48DH480T250A03 ZVS buck-boost described above [n] and a Vicor VTM48EF012T130A01 fixed-ratio Sine Amplitude Converter.[o] One can see from the loop response shown in Figure 11 that the phase margin of the outer loop was 82° and the gain margin was more than 10dB, quite nearly the predicted response, confirming the validity of the model. Across load, the experimental system has a crossover between 49kHz and 66kHz, phase margin of greater than 75° and gain margin of greater than 10dB in all cases.

Figure 11
Loop response, 108A load



Microprocessor power specifications have aggressive criteria for setpoint transient response and tolerance band for step responses; in the case of the Intel VR12 specification, these are 20mV/µs and ±15mV, respectively.[p] Figure 12 shows examples of conformance of this system to these specifications. One may note that the response in each case has minimal ringing and overshoot.

Figure 12
Response to a 1.05 – 1.2V set point transient at 108A load (left) and a 34 – 165A load transient (right)

The compensation parameters are summarized in the following table:

Compensation Attribute	Location in Frequency Domain (kHz)
Integrator Gain-Bandwidth (from Z_F)	1040
Low-Frequency Zero (from Z_F)	30.2
High-Frequency Zero (from Z_I)	90.4
Low-Frequency Pole (from Z_I)	1060
High-Frequency Pole (from Z_F)	2050

Conclusion

There are numerous advantages to using the discontinuous-conduction-mode buck-boost converter as a regulator to power a processor core voltage, though the design offers many challenges. This paper illustrates that these pitfalls can be avoided and a state-of-the art computing power system with outstanding performance can be realized by properly optimizing the AC characteristics of each component in the loop, without the need of sophisticated control strategies or dedicated devices. The example included within this paper can act as a guideline in order to successfully implement the proposed architecture.

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[p] Intel Document, "VR12/IMVP7 Pulse Width Modulation (PWM) Specification," Order Number 397113, October 2011**.**

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